CLAIM AMENDMENTS

Please amend claims 1, 5-30 as follows.

1. (Currently Amended) An apparatus, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having:

a first register coupled to store a first and a second PCI slot operation command, the second PCI slot operation command being different from the first PCI slot operation command; and

a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and second PCI slot operation commands, ~~respectively,~~ the second value being different from the first value.

2. (Original) The apparatus of claim 1, wherein the timing parameter is a time delay between assertion of a signal to control a power state of a target PCI slot and assertion of a signal to control connection of a PCI clock to the target PCI slot.

3. (Original) The apparatus of claim 1, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to a target PCI slot and assertion of a signal to control connection of at least one bus signal to the target PCI slot.

4. (Original) The apparatus of claim 1, wherein the timing parameter is a time delay between assertion or de-assertion of a signal to control a power state of a target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

5. (Original) The apparatus of claim 1, wherein the first and second first and a second PCI slot operation commands are a command to apply power to the target PCI slot, to enable the target PCI slot, to disable the target peripheral card interconnect slot, or to change the speed of the PCI bus.

[5] 6. (Currently Amended) An apparatus, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having:

a first register coupled to store a first and a second PCI slot operation command associated with a first and a second target PCI slot, the second target PCI slot being different from the first target PCI slot; and

a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and the second PCI slot operation commands, ~~respectively,~~ the second value being different from the first value.

[6] 7. (Currently Amended) The apparatus of claim 5, wherein the timing parameter is a time delay between assertion of a signal to control a power state of a target PCI slot and assertion of a signal to control connection of a PCI clock to the target PCI slot.

[7] 8. (Currently Amended) The apparatus of claim 6, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to a target PCI slot and assertion of a signal to control connection of at least one bus signal to the target PCI slot.

[8] 9. (Currently Amended) The apparatus of claim 7, wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of a target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

[9] 10. (Currently Amended) An apparatus, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having:

a first register coupled to store a first and a second PCI slot operation command, the second PCI slot operation command being the same as the first PCI slot operation command; and

a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and the second PCI slot operation commands, ~~respectively,~~ the second value being different from the first value.

[10] 11. (Currently Amended) The apparatus of claim 9, wherein the timing parameter is a time delay between assertion of a signal to control a power state of a target PCI slot and assertion of a signal to control connection of a PCI clock to the target PCI slot.

[11] 12. (Currently Amended) The apparatus of claim 9, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to a target PCI slot and assertion of a signal to control connection of at least one bus signal to the target PCI slot.

[12] 13. (Currently Amended) The apparatus of claim 9, wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of a target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

[13] 14. (Currently Amended) An article of manufacture including a machine-accessible medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving at a first register in [the] a standard hot-plug controller (SHPC) a first value for a timing parameter in a signal sequence for execution of [the] a first peripheral component interconnect (PCI) slot operation command;

receiving at a second register in the ~~a standard hot-plug controller~~ (SHPC) a second ~~first peripheral component interconnect~~ (PCI) slot operation command;

executing the first PCI slot operation command using the signal sequence and the first value for the timing parameter;

receiving at the second register a second PCI slot operation command different from the first PCI slot operation command; and

receiving at the ~~second~~ first register a second value different from the first value for the timing parameter in the signal sequence for execution of the second PCI slot operation command.

[14] 15. (Currently Amended) The article of manufacture of claim 13, wherein the timing parameter is a time delay between assertion of a signal to control a power state of at least one PCI slot and assertion of a signal to control connection of a PCI clock to the at least one target PCI slot using the first and second values.

[15] 16. (Currently Amended) The article of manufacture of claim 13, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to at least one target PCI slot and assertion of a signal to control connection of at least one bus signal to the at least one target PCI slot using the first and second values.

[16] 17. (Currently Amended) The article of manufacture of claim 13, wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of at least one target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

[17] 18. (Currently Amended) The article of manufacture of claim 13, further comprising executing the second PCI slot operation command using the signal sequence and the second value for the timing parameter.

[18] 19. (Currently Amended) An article of manufacture including a machine-accessible medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving at a first register in a standard hot-plug controller (SHPC) a first peripheral component interconnect (PCI) slot operation command associated with a first target PCI slot and receiving at a second register in the SHPC a first value for a timing parameter in a signal sequence for execution of the first PCI slot operation command;

executing the first PCI slot operation command for the first target PCI slot using the signal sequence and the first value for the timing parameter; and

receiving at the first register a second PCI slot operation command associated with a second target PCI slot and receiving at the second register a second value different from the first value for the timing parameter in the signal sequence for execution of the second PCI slot operation command.

[19] 20. (Currently Amended) The article of manufacture of claim 18, wherein the timing parameter is a time delay between assertion of a signal to control a power state of at least one PCI slot and assertion of a signal to control connection of a PCI clock to the at least one target PCI slot using the first and second values.

[20] 21. (Currently Amended) The article of manufacture of claim 18, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to at least one target PCI slot and assertion of a signal to control connection of at least one bus signal to the at least one target PCI slot using the first and second values.

[21] 22. (Currently Amended) The article of manufacture of claim 18, wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of at least one target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

[22] 23. (Currently Amended) The article of manufacture of claim 18, further comprising executing the second PCI slot operation command using the signal sequence and the second value for the timing parameter.

[23] 24. (Currently Amended) An article of manufacture including a machine-accessible medium having data that, when accessed by a machine, cause the machine to perform the operations comprising,

receiving at a first register in [the] a standard hot-plug controller (SHPC) a first value for a timing parameter in a signal sequence for execution of [the] a first peripheral component interconnect (PCI) slot operation command;

receiving at a second register in the ~~a standard hot-plug controller~~ (SHPC) a second ~~first peripheral component interconnect (~~PCI~~)~~ slot operation command;

executing the first PCI slot operation command using the signal sequence and the first value for the timing parameter;

receiving at the second register a second PCI slot operation command the same as the first PCI slot operation command; and

receiving at the first register a second value different from the first value for the timing parameter in the signal sequence for execution of the second PCI slot operation command.

[24] 25. (Currently Amended) The article of manufacture of claim 23, wherein the timing parameter is a time delay between assertion of a signal to control a power state of at least one PCI slot and assertion of a signal to control connection of a PCI clock to the at least one target PCI slot using the first and second values.

[25] 26. (Currently Amended) The article of manufacture of claim 23, wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock to at least one target PCI slot and assertion of a signal to control connection of at least one bus signal to the at least one target PCI slot using the first and second values.

[26] 27. (Currently Amended) The article of manufacture of claim 23, wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of at least one target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command.

[27] 28. (Currently Amended) The article of manufacture of claim 23, further comprising executing the second PCI slot operation command using the signal sequence and the second value for the timing parameter.

[28] 29. (Currently Amended) A system, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having a first register coupled to store a first and a second PCI slot operation command associated with a first and a second target PCI slot, the second target PCI slot being different from the first target PCI slot, and a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and the second PCI slot operation commands, ~~respectively,~~ the second value being different from the first value; and

a static random access memory (SRAM) coupled to the microprocessor.

[29] 30. (Currently Amended) The system of claim 28, further comprising a memory controller coupled to the memory.

[30] 31. (Currently Amended) The system of claim 29, further comprising a software driver coupled to provide the first and the second PCI slot operation commands.